Electronic Version
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Claims

[c1] 1. A multi-chip package, comprising:
a substrate;
a first chip disposed on the substrate;
a plurality of conductive wires electrically connecting the first chip and the substrate;
a package body having a plurality of bumps and electrically connected to the substrate through the bumps; and
a packaging material enclosing the first chip, the conductive wires, the package body and the substrate.

[c2] 2. The multi-chip package of claim 1, wherein the first chip is a functional chip.

[c3] 3. The multi-chip package of claim 1, wherein the package body has a second chip electrically connected to the bumps.

[c4] 4. The multi-chip package of claim 3, wherein the second chip is a memory chip.

[c5] 5. The multi-chip package of claim 3, wherein the packaging material partially encloses the second chip of the package body.

[c6] 6. The multi-chip package of claim 5, further comprising a heat sink attached onto anunenclosed surface of the second chip.

[c7] 7. The multi-chip package of claim 1, further comprising a heat sink attached to the surface of the packaging material.

[c8] 8. The multi-chip package of claim 1, wherein a liquid temperature of the packaging material in an encapsulation processis lower than a melting point of the bumps.

[c9] 9. The multi-chip package of claim 1, wherein the package body further comprises a second chip, a carrier, a plurality of additional bumps and an underfill material layer, the bumps are located between the carrier and the substrate, the additional bumps are located between the second chip and the carrier, the second chip is electrically connected to the substrate via the additional bumps, the carrier and the bumps, and the underfill material layer is filled between the second chip and the carrier and encloses the additional bumps.

[c10] 10. The multi-chip package of claim 1, wherein the package body further comprises a second chip, a carrier, a plurality of additional conductive wires and an additional packaging material, the second chip is disposed

on the carrier, the bumps are located between the carrier and the substrate for electrically connecting the carrier and the substrate, the additional conductive wires electrically connect the second chip with the carrier, and the additional packaging material encloses the second chip, the additional conductive wires and the carrier.

[c11] 11. A process for fabricating a multi-chip package module, comprising the steps of:
providing a substrate;
providing a first chip;
providing a package body having a plurality of bumps;
attaching the first chip to the substrate;
bonding a plurality of conductive wires so that the first chip and the substrate are electrically connected;
bonding the package body to the substrate through the bumps; and
performing an encapsulation process to form a packaging material that encloses the first chip, the conductive wires, the package body and the substrate.

[c12] 12. The process of claim 11, wherein the first chip is a functional chip.

[c13] 13. The process of claim 11, wherein the package body has a second chip electrically connected to the bumps.

[c14] 14. The process of claim 13, wherein the second chip is a memory chip.

[c15] 15. The process of claim 13, wherein the second chip is partially enclosed by the packaging material.

[c16] 16. The process of claim 15, wherein after performing the encapsulation process, a heat sink is attached onto an unenclosed surface of the second chip.

[c17] 17. The process of claim 11, wherein after performing the encapsulation process, a heat sink is attached onto a surface of the packaging material.

[c18] 18. The process of claim 11, wherein after attaching the first chip to the substrate, the conductive wires are bonded to electrically connect the first chip with the substrate, and then the package body is attached to the substrate through the bumps.

[c19] 19. The process of claim 11, wherein after the step of attaching the package body to the substrate through the bumps, the first chip is attached onto the substrate, and then the conductive wires are bonded to electrically connect the first chip with the substrate.

[c20] 20. The process of claim 11, wherein a liquid temperature of the packaging material in the encapsulation pro-

cess is lower than a melting point of the bumps.

[c21] 21. The process of claim 11, wherein the package body further comprises a second chip, a carrier, a plurality of additional bumps and a an underfill material layer, the additional bumps are located between the second chip and the carrier, the second chip is electrically connected to the carrier via the additional bumps, the underfill material layer is filled between the second chip and the carrier and encloses the additional bumps, and after the package body is attached to the substrate through the bumps, the bumps are located between the carrier and the substrate for electrically connecting the carrier and the substrate.

[c22] 22. The process of claim 21, wherein performing the encapsulation process comprises enclosing the second chip of the package body and the carrier of the package body by the packaging material.

[c23] 23. The process of claim 11, wherein the package body further has a second chip, a carrier, a plurality of additional conductive wires and an additional packaging material, the second chip is disposed on the carrier, the additional conductive wires electrically connect the second chip with the carrier, the additional packaging material encloses the second chip, the additional conductive

wires and the carrier, and after the package body is attached to the substrate through the bumps, the bumps are located between the carrier and the substrate for electrically connecting the carrier and the substrate.

[c24] 24. The process of claim 23, wherein after performing the encapsulation process the additional packaging material of the package body and the carrier of the package body are enclosed by the packaging material.